

REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED			
A	Convert to military drawing. Changes to table I. Changes to figures 2 and 4. Editorial changes throughout.										14 April 1987					N A Hauck			
B	Change to table I and figure 1 dimensions.										22 Jan 88					M A Frye			
CURRENT CAGE CODE 67268																			
REV																			
SHEET																			
REV	B	B	B																
SHEET	15	16	17																
REV STATUS OF SHEETS				REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14
Defense Electronics Supply Center Dayton, Ohio Original date of drawing: 4 April 1986 AMSC N/A				PREPARED BY Ray Monnin						MILITARY DRAWING This drawing is available for use by all Departments and Agencies of the Department of Defense									
				CHECKED BY D A Di Cenzo															
				APPROVED BY N A Hauck						TITLE: MICROCIRCUITS, 4 BIT BIPOLAR STATUS AND SHIFT CONTROL UNIT, MONOLITHIC SILICON									
				SIZE A		CODE IDENT. NO. 14933													
				REVISION LEVEL B						DWG NO. 86017									
						SHEET 1 OF 17													

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

<u>86020</u>	<u>01</u>	<u>Q</u>	<u>X</u>
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit</u>
01	2904	4-bit bipolar, status and shift control unit

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
Q	D-5 (40 lead, 9/16" x 2 1/16"), dual-in-line package
Y	See figure 1 (42 lead, 1" x 0.6"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) ^{1/}	1.914 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Case Y	9°C/W
DC output current into inputs	30 mA
DC input current	-30 mA to +5.0 mA
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

^{1/} Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%		Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1.6 mA Y _Z , Y _C , Y _N , Y _{OVR}	1, 2, 3	2.4		V
			I _{OH} = -0.8 mA SIO _o , SIO _n , QIO _o , QIO _n , CT, CO		2.4		V
Output low voltage	V _{OL}	V _{CC} = min, V _{IN} = V _{IH} or V _{IL}	Y _Z , Y _C , Y _N , Y _{OVR}	1, 2, 3		0.5	V
			SIO _o , QIO _o , CT, SIO _n , QIO _n , CO			0.5	V
Input high voltage	V _{IH}	1/		1, 2, 3	2.0		V
Input low voltage	V _{IL}	1/		1, 2, 3		0.8	V
Input clamp voltage	V _{IC}	V _{CC} = min, I _{IN} = -18 mA		1, 2, 3		-1.5	V
Input low current	I _{IL}	V _{CC} = max. V _{IN} = 0.5 V	CP	1, 2, 3		-0.7	mA
			CE _m , CE _μ			-1.8	
			I _Z , I _C , I _N , I _{OVR}			-1.2	
			I _O , I ₁₂ , E _Z , E _C , E _N , E _{OVR} , OE _y , OE _{CT} , CX, Y _Z , Y _C , Y _N , Y _{OVR}			-0.45	
			SE, SIO _o , SIO _n , QIO _o , QIO _n			-1.35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%			Group A subgroups	Limits		Unit
						Min	Max	
Input high current	I _{IH1}	V _{CC} = max V _{IN} = 2.7 V	CP, I ₀ -I ₁₂ , E _Z , E _C , E _N , E _{OVR} , OE _Y , OE _{CT} , C _X CE _m , CE _μ I _Z , I _C , I _N , I _{OVR} , SE SIO _o , SIO _n , QIO _o , QIO _n Y _Z , Y _C , Y _N , Y _{OVR}		1, 2, 3		20 70	μA
Input high current	I _{IH2}	V _{CC} = max, V _{IN} = 5.5 V			1, 2, 3		1.0	mA
Off state (high impedance) output current	I _{OZH} I _{OZL}	V _{CC} = max	CT	V _O = 2.4 V _O = 0.5 SIO _o , SIO _n , QIO _o , QIO _n , 2/ Y _Z , Y _C , Y _N , Y _{OVR} 2/ V _O = 0.5	1, 2, 3		50 -50 110 -1350 70 -450	μA
Output short circuit current 3/	I _{OS}	V _{CC} = 5.75 V, V _O = 0.5 V			1, 2, 3	-30	-85	mA
Power supply 4/	I _{CC}	V _{CC} = max	T _C = -55° C to +125° C		1, 2, 3		348	mA
			T _C = +125° C		2		222	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions $\frac{3}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$ unless otherwise specified $V_{CC} = 5\text{ V} \pm 10\%$	Group A subgroups	Limits		Unit
					Min	Max	
Setup time 1	Inputs: $I_Z, I_{IN},$ I_{OVR}	t_{s1}	$C_L = 50\text{ pF}$, (see figure 4)	9, 10, 11	15		ns
Hold time 1		t_{h1}				5	ns
Setup time 2	Inputs: $I_C (I_1,$ $I_2, I_3 = 001$	t_{s2}			28		ns
Hold time 2		t_{h2}				5	ns
Setup time 3	Inputs: $I_C (I_1,$ $I_2, I_3 \neq 001$	t_{s3}			15		ns
Hold time 3		t_{h3}				5	ns
Setup time 4	Inputs: CE_{μ}	t_{s4}			20		ns
Hold time 4		t_{h4}				3	ns
Setup time 5	Inputs: CE_m	t_{s5}			23		ns
Hold time 5		t_{h5}				4	ns
Setup time 6	Inputs: $E_Z, E_C,$ E_N, E_{OVR}	t_{s6}			23		ns
Hold time 6		t_{h6}				4	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions <u>3/</u> -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%	Group A subgroups	Limits		Unit	
					Min	Max		
Setup time 7	Inputs: I ₀ - I ₅	t _{s7}	C _L = 50 pF, (see figure 4)	9, 10, 11	48		ns	
Hold time 7		t _{h7}				2	ns	
Setup time 8	Inputs: I ₆ - I ₁₀	t _{s8}			44		ns	
Hold time 8		t _{h8}				2	ns	
Setup time 9	Inputs: SE	t _{s9}			40		ns	
Hold time 9		t _{h9}				0	ns	
Setup time 10	Inputs: Y _Z , Y _C , Y _N , Y _{OV} R I ₀ - 5 = LOW	t _{s10}			16		ns	
Hold time 10		t _{h10}				6	ns	
Setup time 11	Inputs: SI ₀ , SI ₀ _n , QI ₀ , QI ₀ _n	t _{s11}			20		ns	
Hold time 11		t _{h11}				5	ns	
Propagation delay 1: From (input): I _Z , I _C , I _N , I _{OV} R, To (output): Y _Z , Y _C , Y _N , Y _{OV} R		t _{pd1}					40	ns
Propagation delay 2: From (input): CP To (output): Y _Z , Y _C , Y _N , Y _{OV} R		t _{pd2}					45	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>3/</u> -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay 3: From (input): I ₄ , I ₅ To (output): Y _Z , Y _C , Y _N , Y _{OV} R	t _{pd3}	C _L = 50 pF, (see figure 4)	9, 10, 11		38	ns
Propagation delay 4: From (input): I _Z , I _C , I _N , I _{OV} R To (output): CT	t _{pd4}				44	ns
Propagation delay 5: From (input): CP To (output): CT	t _{pd5}				40	ns
Propagation delay 6: From (input): I ₀ - I ₅ To (output): CT	t _{pd6}				41	ns
Propagation delay 7: From (inputs): CX To (outputs): CO	t _{pd7}				22	ns
Propagation delay 8: From (inputs): CP To (outputs): CO	t _{pd8}				28	ns
Propagation delay 9: From (inputs): I ₁ , I ₂ , I ₃ , I ₅ , I ₁₁ , I ₁₂ To (outputs): CO	t _{pd9}				42	ns
Propagation delay 10: From (inputs): SIO _n , QIO _n To (output): SIO _o	t _{pd10}				20	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay 11: From (inputs): SIO _O , QIO _O To (output): SIO _n	t _{pd11}	C _L = 50 pF, (see figure 4)	9, 10, 11		20	ns
Propagation delay 12: From (inputs): I _C , I _N , I _{OV} R To (output): SIO _n	t _{pd12}				29	ns
Propagation delay 13: From (inputs): SIO _n , QIO _n To (output): QIO _O	t _{pd13}				20	ns
Propagation delay 14: From (inputs): SIO _O , QIO _O To (output): QIO _n	t _{pd14}				20	ns
Propagation delay 15: From (input): CP To (outputs): SIO _O , SIO _n , QIO _O , QIO _n	t _{pd15}				32	ns
Propagation delay 16: From (inputs): I ₆ - I ₁₀ To (outputs): SIO _O , SIO _n , QIO _O , QIO _n	t _{pd16}				31	ns
Enable time 1: From (input): OE _{CT} To (output): CT	t _{EN1}				25	ns
Disable time 1: From (input): OE _{CT} To (output): CT	t _{DIS1}	C _L = 5 pF (see figure 4)	9,10,11		18	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{3/} -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%	Group A subgroups	Limits		Unit
				Min	Max	
Enable time 2: From (input): SE To (outputs): SIO _O , SIO _N , QIO _O , QIO _N	t _{EN2}	C _L = 50 pF, (see figure 4)	9, 10, 11		35	ns
Disable time 2: From (input): SE To (outputs): SIO _O , SIO _N , QIO _O , QIO _N	t _{DIS2}	C _L = 5 pF (see figure 4)			20	ns
Enable time 3: From (input): I ₁₀ To (outputs): SIO _O , SIO _N , QIO _O , QIO _N	t _{EN3}	C _L = 50 pF (see figure 4)			43	ns
Disable time 3: From (input): I ₁₀ To (outputs): SIO _O , SIO _N , QIO _O , QIO _N	t _{DIS3}	C _L = 5 pF (see figure 4)			32	ns
Enable time 4: From (input): OE _y To (outputs): Y _Z , Y _C , Y _N , Y _{OVR}	t _{EN4}	C _L = 50 pF (see figure 4)			28	ns
Disable time 4: From (input): OE _y To (outputs): Y _Z , Y _C , Y _N , Y _{OVR}	t _{DIS4}	C _L = 5 pF (see figure 4)			23	ns
Enable time 5: From (inputs): I ₀ - I ₅ To (outputs): Y _Z , Y _C , Y _N , Y _{OVR}	t _{EN5}	C _L = 50 pF (see figure 4)			30	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{3/} -55° C ≤ T _C ≤ +125° C unless otherwise specified V _{CC} = 5 V ±10%	Group A subgroups	Limits		Unit
				Min	Max	
Disable time 5: From (inputs): I ₀ -I ₅ To (outputs): Y _Z , Y _C , Y _N , Y _{OVR}	t _{DIS5}	C _L = 5 pF, (see figure 4)	9, 10, 11		41	ns
Minimum clock low time	t _{CL}			25		ns
Minimum clock high time	t _{CH}			25		ns

- 1/ These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).
- 2/ These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with output enables high.
- 3/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
- 4/ Worst case I_{CC} is at minimum temperature.

3.8 Verification and review. DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

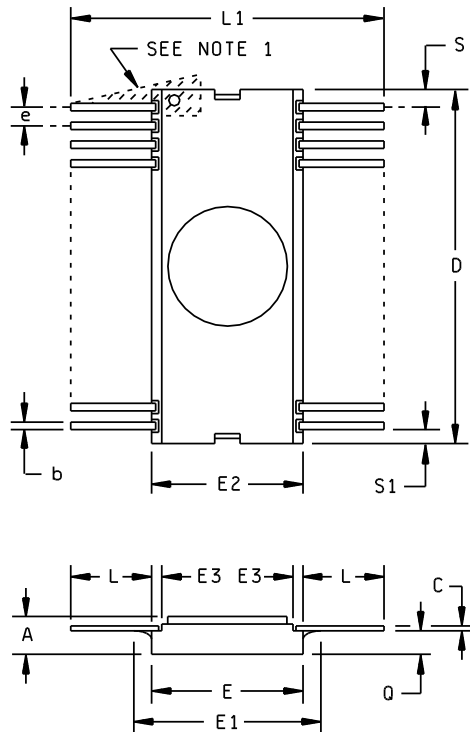
4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) T_A = +125° C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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PARAMETER	MIN.	MAX.
A	.070	.098
b	.017	.023
c	.006	.010
D	1.050	1.090
E	.620	.660
E1	----	.720
E2	.520	----
E3	.030	----
e	.045	.055
L	.310	.370
L1	1.280	1.360
Q	.030	.060
S	----	.045
S1	.005	----

NOTES:

1. Index area: A notch, tab, or pin identification mark shall be located within the shaded area shown.
2. E1 allows for Ag-Cu alloy brazed overrun.
3. Dim. b and c increase by 3 mils max. limit if tinplate/solder dip lead finish is applied.
4. All dimensions are given in inches.

FIGURE 1. Case outline Y.

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CONNECTOR DIAGRAM
TOP VIEW

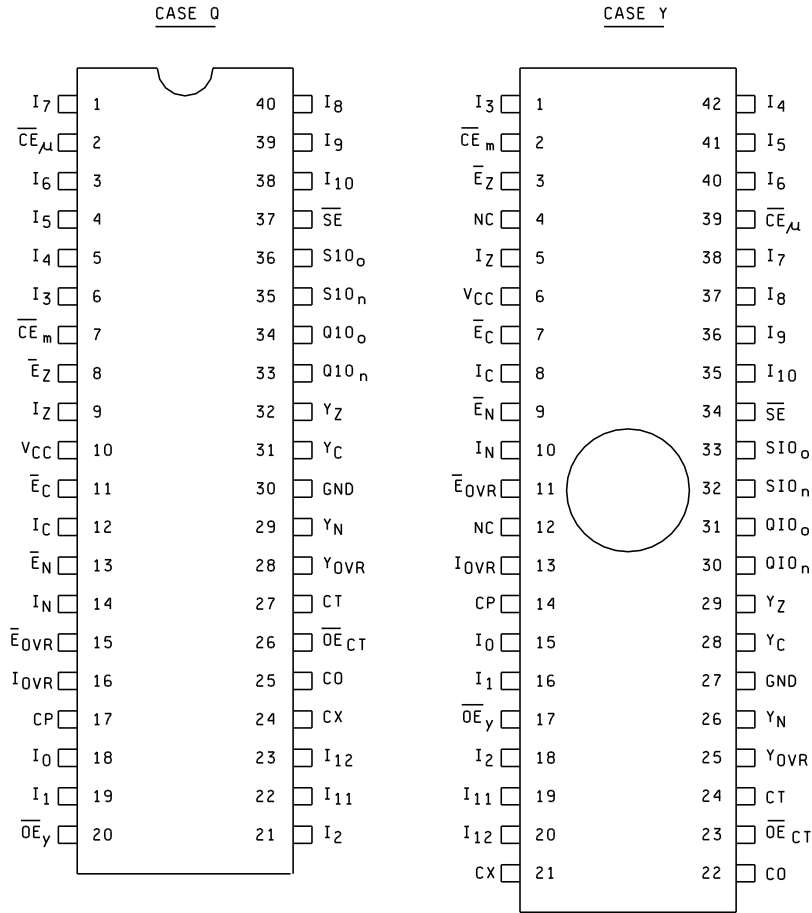


FIGURE 2. Terminal connections.

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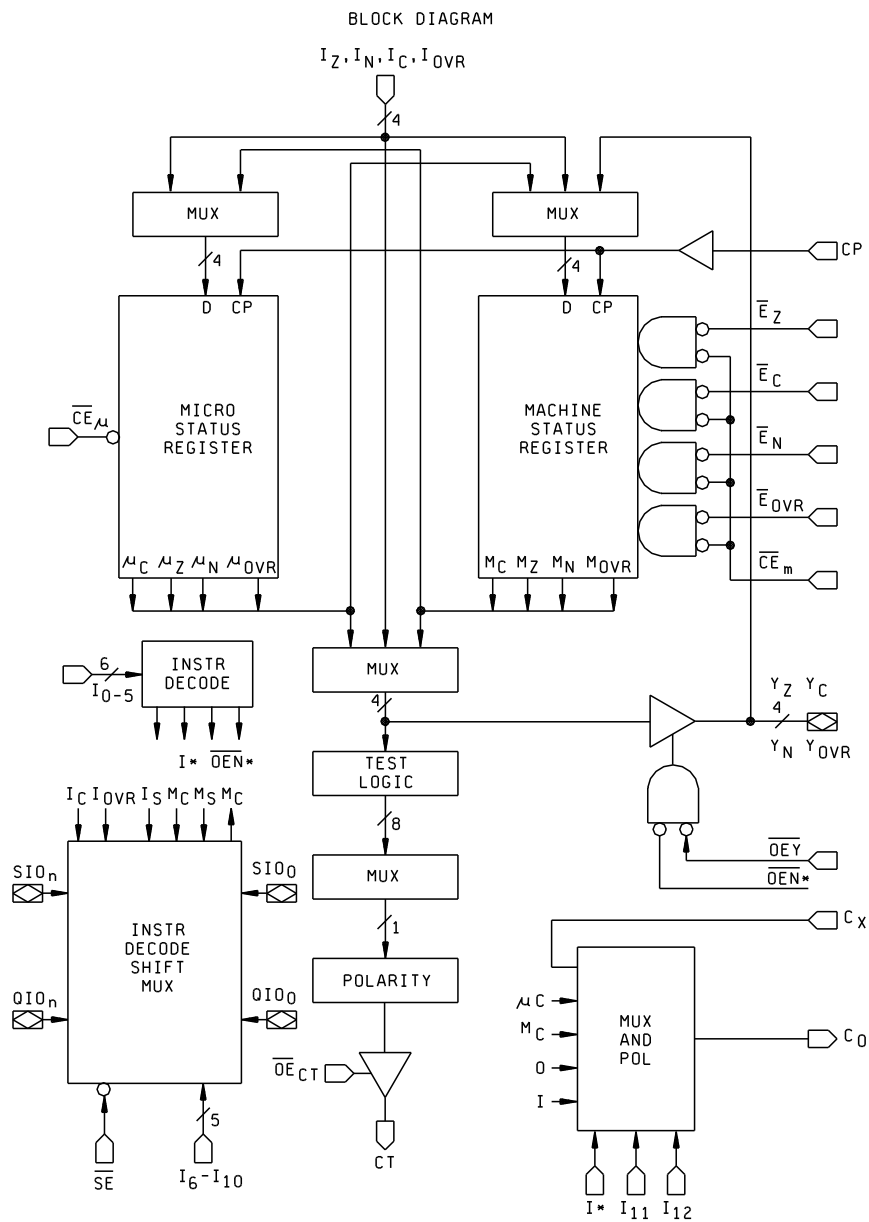


FIGURE 3. Functional block diagram.

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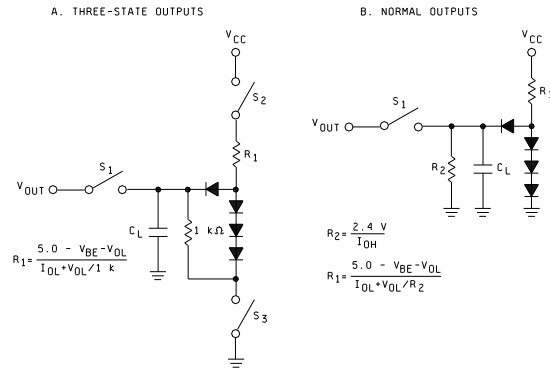
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SWITCHING TEST CIRCUIT



Pin (DIP)	Pin (FP)	Pin label	Test circuit	R ₁	R ₂
25	22	CO	B	470	3k
27	24	CT	A	430	1k
28	25	Y _{OVR}	A	220	1k
29	26	Y _N	A	220	1k
31	28	Y _C	A	220	1k
32	29	Y _Z	A	220	1k
33	30	QIO _n	A	430	1k
34	31	QIO _O	A	430	1k
35	32	SIO _n	A	430	1k
36	33	SIO _O	A	430	1k

NOTES:

1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S₁, S₂, and S₃ are closed during function tests and all ac tests except output enable test.
3. S₁, S₂, and S₃ are closed S₁, while S₂ is open for t_{PHZ} test. S₁ and S₂ are closed while S₃ is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

FIGURE 4. Load circuit.

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4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 must verify input to output logic combinations.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-6375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
8601701QX	34335	AM2904/BQA
8601701YX	34335	AM2904/BYC

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34335

Vendor name
and address

Advanced Micro Devices, Inc.
901 Thompson Place
P.O. Box 3453
Sunnyvale, CA 94088

**STANDARDIZED
MILITARY DRAWING**
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

86017

REVISION LEVEL
B

SHEET
17